REMARKS

A Request for Continued Examination (RCE) (and fee) and an Excess Claim Fee Payment Letter for an excess independent claim are being filed concurrently herewith including a request for entry of the Amendment filed on August 14, 2002.

Claims 3-5, 11-18, 20-22, and 24-31 are all the claims pending in the application. Claims 6-9 have been canceled and new claims 26-31 have been added above.

Applicant points out that in a non-limiting embodiment of the present invention, two transistors are provided which include source regions or drain regions coupled to each other on one semiconductor chip, and each transistor may have a two or three forked gate electrode. In more detail, each transistor may have a gate electrode layer which is electrically separate from the other. Further, the transistors may be arranged next to each other.

In contrast, in a conventional technique, it is taken for granted that source regions or drain regions of these transistors are commonly used as shown in the conventional art of Fig. 7 of Applicant's specification, or source regions or drain regions of those transistors are arranged next to each other as shown in the conventional art of Fig. 6 of Applicant's specification to reduce an arranged area.

However, as described in the "Description of the Related Art" section of the specification, the two transistors in such an arrangement include a disadvantage of having unequal electrical capabilities with respect to each other when a mask for forming contact holes reaching the source regions or drain regions is misaligned (e.g., see specification, page 2, line 1-21). This is a problem for two transistors which may work together to perform a function. To address and solve this problem, the present invention, in a non-limiting embodiment of the invention, purposely arranges source regions or drain regions in a particular order as defined by the claims.

On the other hand, Bush only shows one transistor having a four forked gate electrode and does not disclose or suggest how to arrange two transistors when they are formed on one chip. Also, Ham only discloses one transistor having a six forked gate electrode.

Therefore, even if two transistors, whose source regions or drain regions are coupled to each other on one semiconductor chip, were formed by one of ordinary skill in the art at the time of invention, these transistors would be arranged similar to the arrangement of the transistors described in the conventional art of the present invention.

Further, Mizuno, Lin, and/or Uehara, either alone or in combination with each other or Bush, and/or Ham, do not teach or suggest the features of the present invention.

In view of the above, Applicant submits that all of claims 3-5, 11-18, 20-22, and 24-31 are patentable over the cited references.

Early, favorable prosecution on merit is respectfully requested.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

Respectfully submitted,

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